Amendments to the Specification:

Please replace the paragraph beginning at page 3, line 20, with the following amended paragraph:

In the data line driver circuit, a shift ~~resister~~ register may have the maximum operating frequency shown in Fig. 9 or 10. For example, each of the TFTs of the data line driver circuit has a maximum operating frequency of 16MHz with a channel length 4 μm, and of 1GHz with a channel length of 1.5 μm.

Please replace the paragraph bridging at pages 4 and 5 with the following amended paragraph:

Fig. 9 is a graph showing an operational characteristic of a shift ~~resister~~ register in the liquid crystal display device of active matrix type according to Embodiment 1 of the semiconductor display device of the present invention;

Please replace the paragraph beginning at page 5, line 2, with the following amended paragraph:

Fig. 10 is a graph showing an operational characteristic of a shift ~~resister~~ register in the liquid crystal display device of active matrix type according to Embodiment 1 of the semiconductor display device of the present invention;

Please replace the paragraphs beginning at page 6, line 5, with the following amended paragraphs:

Reference numeral 101 denotes a data line driver circuit. The data line driver circuit 101 has a shift ~~resister~~ register 1011, a level shifter 1012 and a buffer 1013. As for signals to be inputted to the data line driver circuit 101, as shown in Fig. 1, CLK (clock), CLKb (inverted clock), SP (start pulse), Vdd (+2V power supply), VddH (+8V power supply) and Vss (-8V power supply) are included.

Reference numeral 102 denotes a left hand scanning line driver circuit, and 103 denotes a right hand scanning line driver circuit. The scanning line driver circuits 102 and 103 have the identical structure to each other, and both of them receive the same signals. This is employed with the intention of eliminating stagnation of scanning signals by simultaneously driving the scanning lines with both of the left and the right circuits, and, as well, of taking precautions against such a case that either the left circuit or the right circuit would not operate. The scanning line driver circuit 102 has a shift ~~resister~~ register 1021, a level shifter 1022 and a buffer 1023. The scanning line driver circuit 103 has a shift ~~resister~~ register 1031, a level shifter 1032 and a buffer 1033. As for signals to be inputted to the left hand scanning line driver circuit 102 and the right hand scanning line driver circuit 103, CLK (clock), SP (start pulse), Vdd (+2V power supply), VddH (+8V power supply) and Vss (-8V power supply) are included.

Please replace the paragraphs beginning at page 7, line 8, with the following amended paragraphs:

Next, reference will be made to Fig. 2. Fig. 2 is a circuit diagram showing the data line driver circuit 101 according to this embodiment of the present invention. The shift ~~resister~~ register 1011, as shown in Fig. 2, has as its components an SR 1, an SR 2,····· and an SR 160. Each of the components has an inverter 10112 and a clocked inverter 10113. Reference numeral 10111 denotes an inverter for buffering a start pulse.

A timing signal supplied from each of the components SR 1, SR 2,····· and SR 160 of the shift ~~resister~~ register 1011 is supplied to the level shifter 1012 through NAND

circuit (NAND 1, NAND 2, ····· and NAND 160). The timing signal to be inputted to and outputted from the NAND circuit and the shift ~~resister~~ register 1011 is 10 V, which is increased to 16 V by the level shifter 1012.

Please replace the paragraphs beginning at page 16, line 1, with the following amended paragraphs:

Next, reference is made to Figs. 9 and 10. Shown in Figs. 9 and 10 are characteristics in operating frequency of the shift ~~resister~~ register 1011 when the liquid crystal display device of active matrix type is manufactured by the fabricating method in accordance with the present invention. Fig. 9 takes up the case where the channel length of each of the P channel type TFT and N channel type TFT is 4 μm, which constitutes the shift ~~resister~~ register 1011, while Fig. 10 takes up the case of 1.5 μm.

Fig. 9 indicates that the shift ~~resister~~ register operates at about 0.5 MHz at the maximum when the applied voltage is 3V. If the applied voltage is 4V, it operates at about 2 MHz at the maximum; when 5V, about 5 MHz at the maximum; when 6V, about 9 MHz at the maximum; when 7V, about 11 MHz at the maximum; when 8V, about 13 MHz at the maximum; when 9V, about 16 MHz at the maximum.

Fig. 10 teaches that the shift ~~resister~~ register operates at about 20 and several MHz at the maximum when the applied voltage is 4V. If the applied voltage is 5V, it operates at about 40 and several MHz at the maximum; when 6V, about 60 and several MHz at the maximum; when 7V, about 70 and several MHz at the maximum; when 8V, about 80 and several MHz at the maximum; when 8.5V, nearly 100 MHz at the maximum. Therefore, the drawings persuasively shows that high speed drive is realized with the liquid crystal display device of active matrix type manufactured by the fabricating method in accordance with the present invention.

Fig. 11 is a photograph showing a pattern of the data line driver circuit 101 in the liquid crystal display device of active matrix type of this embodiment. It can be

understood that the shift ~~resister~~ register 1011, NAND circuit, the level shifter 1012 and the buffer 1013 are formed.